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<u>L25</u>	L22 and l8	22	<u>L25</u>
<u>L24</u>	L22 and l7	41	<u>L24</u>
<u>L23</u>	L22 and l6	76	<u>L23</u>
<u>L22</u>	predict\$5 near8 branch\$4 near25 cach\$3 near15 way\$1	101	<u>L22</u>
<u>L21</u>	predict\$5 near8 branch\$4 near25 cach\$3	1864	<u>L21</u>
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<u>L20</u>	l3 and l3	16	<u>L20</u>
<u>L19</u>	l3 and l7	7	<u>L19</u>
<u>L18</u>	l3 and l6	11	<u>L18</u>
<u>L17</u>	l5 and l8	5	<u>L17</u>
<u>L16</u>	l5 and l7	20	<u>L16</u>

<u>L15</u>	15 and 16	27	<u>L15</u>
<u>L14</u>	14 and 18	8	<u>L14</u>
<u>L13</u>	14 and 17	39	<u>L13</u>
<u>L12</u>	14 and 16	52	<u>L12</u>
<u>L11</u>	12 and 18	8	<u>L11</u>
<u>L10</u>	12 and 17	36	<u>L10</u>
<u>L9</u>	12 and 16	49	<u>L9</u>
<u>L8</u>	(711/130-153)[CCLS]	8194	<u>L8</u>
<u>L7</u>	(712/235,236,239,240)[CCLS]	888	<u>L7</u>
<u>L6</u>	(712/2-300)[CCLS]	12232	<u>L6</u>
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<u>L5</u>	L4 and (dependen\$5 or conflict\$4 or contend\$4 or contention\$1 or hazard\$4 or collaps\$5)	36	<u>L5</u>
<u>L4</u>	(section\$1 or region\$1 or area\$1 or bank\$1 or portion\$1 or segment\$1) near12 memor\$4 near55 predict\$5 near6 branch\$4	74	<u>L4</u>
<u>L3</u>	L2 and (conflict\$4 or contend\$4 or contention\$1 or hazard\$4 or collaps\$5)	17	<u>L3</u>
<u>L2</u>	(section\$1 or region\$1 or area\$1 or bank\$1 or portion\$1 or segment\$1) near12 memor\$4 near25 predict\$5 near6 branch\$4	71	<u>L2</u>
<u>L1</u>	bank\$1 near12 memor\$4 near25 predict\$5 near6 branch\$4	7	<u>L1</u>

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IEEE JNL IEEE Journal or Magazine

IEEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

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Patt, Y.N.; Patel, S.J.; Evers, M.; Friendly, D.H.; Stark, J.;

[Computer](#)

Volume 30, Issue 9, Sept. 1997 Page(s):51 - 57

Digital Object Identifier 10.1109/2.612249

[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(328 KB) IEEE JNL[Rights and Permissions](#)**2. An architectural framework for runtime optimization**

Merten, M.C.; Trick, A.R.; Barnes, R.D.; Nystrom, E.M.; George, C.N.; Gyllenhaal, J.C.; Hwu, W.-M.

[Computers, IEEE Transactions on](#)

Volume 50, Issue 6, June 2001 Page(s):567 - 589

Digital Object Identifier 10.1109/12.931894

[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(3812 KB) IEEE JNL[Rights and Permissions](#)**3. Software Trace Cache**

Ramirez, A.; Larriba-Pey, J.L.; Valero, M.;

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Volume 54, Issue 1, Jan 2005 Page(s):22 - 35

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[AbstractPlus](#) | Full Text: [PDF](#)(1032 KB) IEEE JNL[Rights and Permissions](#)**4. Deep jam: conversion of coarse-grain parallelism to instruction-level and vector parallelism applications**

Carribault, P.; Cohen, A.; Jalby, W.;

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17-21 Sept. 2005 Page(s):291 - 300

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Hill, M.D.; Falsafi, B.; Wood, D.A.; Mukherjee, S.S.;

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